

SELECTIVE ELECTROLESS-PLATED COPPER METALLIZATION

Related Applications

This application is related to the following co-filed and commonly assigned
5 applications; attorney docket number 303.618US1, entitled "Method and Apparatus
for Making Integrated-Circuit Wiring from Copper, Silver, Gold, and Other Metals," S/N: 09/488 098
and attorney docket number 303.648US1, entitled "Method for Making Copper
Interconnects in Integrated Circuits," which are hereby incorporated by reference. In 4-4-03
S/N: 09/484 303

10 Field of the Invention

The present invention relates generally to integrated circuits. More particularly, it pertains to structures and methods for selective electroless-plated copper metallization.

15 Background of the Invention

The rapid progress in miniaturization of integrated circuits (IC) is leading to denser and finer pitched chips with ever increasing performance. In order to enhance the performance of advanced ICs, the interconnect systems are gradually migrating from aluminum-based metallurgy to higher-conductivity and more
20 electromigration-resistant copper. Of the several schemes proposed for fabricating copper interconnects, the most promising method appears to be the Damascene process. Using this method, the trenches and vias are patterned in blanket dielectrics, and then metal is deposited into the trenches and holes in one step, followed by chemical mechanical polishing (CMP) to remove the unwanted surface
25 metal. This leaves the desired metal in the trenches and holes, and a planarized surface for subsequent metallization. During the CMP process, especially for the via holes, more than 99% of the deposited copper is removed, and this is a very wasteful and expensive process, which includes a high usage of consumables such as pads and slurry. Furthermore, the disposition of used materials is a very

important environmental issue. Therefore it is highly desirable to accomplish the copper metallization without CMP.

One approach to the formation of copper vias and metal lines includes the electroless deposition of copper. Electroless deposition of copper is used in printed circuit boards to manufacture copper lines and through holes where the line and hole dimensions are in the several tens to hundreds of microns. This is, of course, much larger than the sub-micron design rules for integrated circuit fabrication on silicon wafers. In this approach, Palladium (Pd) is often used as the activated base metal for electroless copper plating. Several different groups have shown the success of the same. For example, an article published by Bhansali and D.K. Sood, entitled, "A novel technique for fabrication of metallic structure on polyimide by selective electroless copper plating using ion implantation," Thin Solid Films, vol. 270, p. 489-492, 1995, successfully used palladium ion implantation into polyimide to seed an electroless plated copper film on the polyimide surface. An ion dose range of 1.5×10^{15} to 1.2×10^{17} ions/cm² was used. They also reported on the successful use of copper implantation into silicon to seed the electroless plating using a dose range of 5×10^{14} to 6.4×10^{16} ions/cm². (See, Bhansali, S. et al, "Selective electroless copper plating on silicon seeded by copper ion implantation", Thin Solid Films, vol. 253, no. 1-2, p. 391-394, 1994). An article published by M.-H. Kiang, et al, entitled, "Pd/Si plasma immersion ion implantation for selective electroless copper plating on SiO₂, Applied Physics Letters, vol. 60, no. 22, p. 2767-2769, 1992, demonstrated selective deposition of copper in SiO₂ trenches using Pd/Si plasma immersion ion implantation and electroless copper plating. An article published by J.-Y. Zhang et al, entitled, "Investigations of photo-induced decomposition of palladium acetate for electroless copper plating", Thin Solid Films, vol. 318, p. 234-238, 1998, illustrates photo-induced palladium decomposition of acetate performed by using argon and xenon excimer vacuum ultraviolet sources in the formation of palladium, which acted as a catalyst for subsequent copper plating by means of an electroless bath for selective copper deposition. An article published by M.-H. Bernier et al, entitled,

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“Laser processing of palladium for selective electroless copper plating”, SPIE Proc., vol. 2045, p. 330-337, 1993 demonstrated that the direct writing of palladium features by the Ar⁺ laser-induced pyrolytic decomposition of an organometallic palladium resins on polyimide and Si₃N₄ led to active Pd sites which were

5 selectively copper plated. Also, as described in an article published by J.-L. Yeh et al, entitled, “Selective Copper Plating of Polysilicon surface Micromachined Structures”, Technical digest of 1998 Solid-State Sensor and Actuator Workshop, Transducer Research Foundation Catalog No. 98TRF-0001, p.248-251, 1998, Yeh et al. exposed polycrystalline silicon structures to a palladium solution that selectively

10 activated the polysilicon structure, but not the silicon oxide or nitride layers. Upon immersion into a copper plating solution at a temperature between 55 and 80° C, the copper nuclei were initially formed on the Pd+ activated polysilicon surface. After the formation of a thin-layer copper, copper started to deposit on this thin initiated copper film. Recently, an article published by V.M. Dubin et al, entitled, “Selective

15 and Blanket Electroless Copper Deposition for Ultralarge Scale Integration”, J. Electrochem. Soc., vol. 144, no. 3, p. 898-908, 1997, disclosed a novel seeding method for electroless copper deposition on sputtered copper films with an aluminum protection layer. This seeding method consisted of (i) deposition of Cu seed layer by sputtering or evaporation, (ii) deposition of a sacrificial thin aluminum

20 layer without breaking vacuum, (iii) etching the aluminum layer in the electroless Cu plating bath, followed by electroless Cu deposition.

Here, Dubin et al. designed and constructed a single-wafer electroless copper deposition tool with up to 200 mm wafer capability, and an electroless copper deposition process was developed. Electroless Cu films deposited at high plating

25 rate (up to 120 nm/min) in solutions with optimized plating chemical environment exhibited low resistivity (<2 μ ohm cm for as deposited films), low surface roughness, and good electrical uniformity.

All of these above described methods are rather complex which means that the number of process steps involved in integrated circuit fabrication increases. The

problem associated with these methods is that an increase in the number of process steps makes integrated circuit fabrication more costly. Further, none of the above described methods address or provide a resolution to the costly excess expenditure of materials and the environmental concerns when such processes are implemented to form sub-micron vias and metal lines on wafers in a conventional CMP fabrication process.

For the reasons stated above and for others which will become apparent from reading the following disclosure, structures and methods are needed which alleviate the problems associated with via and metal line fabrication processes. These structures and methods for via and metal line fabrication must be streamlined and accommodate the demand for higher performance in integrated circuits even as the fabrication design rules shrink.

Summary of the Invention

The above mentioned problems associated with integrated circuit size and performance, the via and metal line formation process, and other problems are addressed by the present invention and will be understood by reading and studying the following specification. Structures and methods are provided which include a selective electroless copper metallization. The present invention provides for a multilayer copper wiring structure by electroless, selectively deposited copper in a streamlined process which will not require chemical mechanical planarization (CMP). Thus, the present invention significantly reduces the amount of deposited conductive material, e.g. copper, which is ultimately discarded according to conventional processes. This alleviates important environmental concerns regarding the disposition of used materials. Further, by avoiding the need for a CMP process step, the usage of consumables such as pads and slurry is conserved.

In particular, an illustrative embodiment of the present invention includes a novel methodology for forming copper vias on a substrate. This method includes depositing a thin film seed layer of Palladium (Pd) or Copper (Cu) on a substrate.

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The seed layer is deposited to a thickness of less than 15 nanometers (nm). A photolithography technique is used to define a number of via holes above the seed layer. In one embodiment, using a photolithography technique includes forming a patterned photoresist layer to define the number of via holes above the seed layer. A layer of copper is deposited over the seed layer using electroless plating filling the number of via holes to a top surface of the patterned photoresist layer. The method can be repeated any number of times depositing a second seed layer, depositing another patterned photoresist layer defining a number of conductor line openings above the second seed layer, and forming a second layer of copper using electroless plating which fills the number of conductor line openings to a top surface of the second patterned photoresist layer. The photoresist layers along with the seed layers in other regions can then be removed by ashing and a chemical mechanical planarization process is avoided. Structures formed by this novel process are similarly included within the scope of the present invention.

These and other embodiments, aspects, advantages, and features of the present invention will be set forth in part in the description which follows, and in part will become apparent to those skilled in the art by reference to the following description of the invention and referenced drawings or by practice of the invention. The aspects, advantages, and features of the invention are realized and attained by means of the instrumentalities, procedures, and combinations particularly pointed out in the appended claims.

Brief Description of the Drawings

The following detailed description of the preferred embodiments can best be understood when read in conjunction with the following drawings, in which:

Figures 1A-1B illustrate an embodiment of the various processing steps for forming vias and metal lines according to the teachings of the prior art;

Figures 2A-2K illustrate an embodiment of the various processing steps for a selective electroless-plated copper metallization according to the teachings of the present invention.

Figure 3 is an illustration of an integrated circuit formed according to the teachings of the present invention.

Detailed Description

In the following detailed description of the invention, reference is made to the accompanying drawings which form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention.

The terms wafer and substrate used in the following description include any structure having an exposed surface with which to form the integrated circuit (IC) structure of the invention. The term substrate is understood to include semiconductor wafers. The term substrate is also used to refer to semiconductor structures during processing, and may include other layers that have been fabricated thereupon. Substrate include doped and undoped semiconductors, epitaxial semiconductor layers supported by a base semiconductor or insulator, as well as other semiconductor structures well known to one skilled in the art. The term insulator is defined to include any material that is less electrically conductive than the materials generally referred to as conductors by those skilled in the art. The following detailed description is, therefore, not to be taken in a limiting sense.

Figures 1A-1B illustrate an embodiment of the various processing steps for forming vias and metal lines according to the teachings of the prior art. As shown in Figure 1A, a number of vias 101-1 and 101-2 are formed in an insulator material 103, e.g. silicon dioxide (SiO_2), contacting with a substrate 100. As one of ordinary

skill in the art will recognize, any number of semiconductor devices can be formed in the substrate to which the number of vias 101-1 and 101-2 make electrical contact.

Conventionally, to form vias and aluminum wire metal lines, fabricators use a dual-damascene metallization technique, which takes its name from the ancient Damascene metalworking art of inlaying metal in grooves or channels to form ornamental patterns. The dual-damascene technique entails covering the components on a wafer with an insulative layer 103, etching small holes in the insulative layer 103 to expose portions of the components underneath in substrate 100, and subsequently etching shallow trenches from hole to hole to define a number of metal lines. Fabricators then blanket the entire insulative layer with a layer of aluminum or other conductive material and polish off the excess, leaving behind conductive vias, or contact plugs, in the holes and conductive lines in the trenches.

As shown in the prior art of Figure 1A, a layer of copper 104 can be deposited in the holes and trenches using an electroplated copper deposition technique. As shown in Figure 1A, the copper layer 104 fills the holes and the trenches, but also covers all of the surfaces features such the insulator material 103 used in the dual damascene process.

Figure 1B illustrates the structure after the excess copper has been removed through a chemically mechanical planarization (CMP) process step. As shown in the prior art Figure 1B, the CMP process step polishes the deposited layer of copper 104 down to and level with the top surface of the insulator layer 103 to form the copper vias 101-1 and 101-2 as well as copper metal lines 105-1 and 105-2. One of ordinary skill in the art will understand, upon viewing the fabrication process illustrated in Figures 1A and 1B, the wastefulness in the amount of copper which is discarded in the CMP process step.

Method of the Present Invention



Figures 2A through 2K illustrate a novel methodology for a selective electroless-plated copper metallization according to the teachings of the present invention. Specifically, Figure 2A through 2K illustrate a method for forming a multilayer copper (Cu) wiring structure on a substrate. The methodology of the present invention avoids the need for a chemical mechanical planarization (CMP) process step in forming the same. As shown in Figure 2A, a seed layer, or first seed layer, 202 is deposited on a substrate 200. In one embodiment, depositing the first seed layer 202 on the substrate 200 includes depositing a thin film of Palladium (Pd) on the substrate 200. In another embodiment, depositing the first seed layer 202 on the substrate 200 includes depositing a thin film of Copper (Cu) on the substrate. The seed layer 202 is deposited to have a thickness of less than 15 nanometers (nm). In one exemplary embodiment, the seed layer 202 is deposited to form a barely continuous film in the thickness range of 3 to 10 nm. In another exemplary embodiment, the seed layer 202 is deposited such that the seed layer possesses a discontinuous island structure in the thickness range of 3 to 10 nm. In one embodiment, the seed layer 202 is deposited using a physical vapor deposition process. For example, in one embodiment, the seed layer 202 is deposited using a sputtering deposition technique. In another embodiment, the seed layer 202 is deposited using an evaporation deposition technique. One of ordinary skill in the art will understand, upon reading this disclosure, the manner in which such physical vapor deposition processes can be performed to form the seed layer 202 described herein.

Figure 2B illustrates the structure following the next sequence of processing steps. In Figure 2B, a photolithography technique is used to define a number of via holes, or openings, 206-1, 206-2, . . . , 206-N, above the seed layer 202 on the substrate 200. As one of ordinary skill in the art will understand upon reading this disclosure, using a photolithography technique to define a number of holes 206-1, 206-2, . . . , 206-N, includes patterning a photoresist layer 208 to define the number via holes, or openings, 206-1, 206-2, . . . , 206-N over the seed layer 202. One of

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ordinary skill in the art will also understand upon reading this disclosure, the manner of forming the patterned photoresist layer, or first patterned photoresist layer, 208. For example, a photoresist layer can be deposited over the seed layer 202 using any suitable technique, e.g. by spin coating. Then the photoresist can be masked, 5 exposed, and washed to define the number of via holes, or openings, 206-1, 206-2, . . . , 206-N to the seed layer 202. One of ordinary skill in the art will further understand, upon reading this disclosure, that the thickness of the photoresist layer 202 is scalable. That is, the deposition of the photoresist layer 208 is controllable such that the photoresist thickness can be set at a predetermined height (h1). Thus, 10 the scalable thickness of the photoresist layer 208 determines a height (h1), or depth (h1) for the number of via holes, or openings, 206-1, 206-2, . . . , 206-N. The structure is now as appears in Figure 2B.

Figure 2C illustrates the structure following the next sequence of processing steps. In Figure 2C, a layer of copper, first layer of copper, or first level of copper 15 vias 210 is deposited over the seed layer 202 using electroless plating. One of ordinary skill in the art will understand upon reading this disclosure the various manner in which the layer of copper, first layer of copper, or first level of copper vias 210 can be deposited over the seed layer 202 using electroless plating. According to the teachings of the present invention, the layer of copper, first layer of 20 copper, or first level of copper vias 210 is formed in the number of via holes, or openings, 206-1, 206-2, . . . , 206-N. Forming layer of copper, first layer of copper, or first level of copper vias 210 includes filling the number of via holes, or openings, 206-1, 206-2, . . . , 206-N to a top surface 214 of the first patterned photoresist layer 208. According to the teachings of the present invention 25 depositing the layer of copper, first layer of copper, or first level of copper vias 210 over the seed layer 202 is such that the layer of copper, first layer of copper, or first level of copper vias 210 form on the seed layer 202 but not on the patterned photoresist layer 208. The structure is now as appears in Figure 2C.

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Figure 2D illustrates the structure following the next sequence of processing steps. In Figure 2D, another seed layer, or second seed layer, 216 is deposited on the first layer of copper, or first level of copper vias 210 and the top surface 214 of the first patterned photoresist layer 208. In one embodiment, depositing the second seed layer 216 on the first layer of copper, or first level of copper vias 210 and the top surface 214 of the first patterned photoresist layer 208 includes depositing a thin film of Palladium (Pd). In another embodiment, depositing the second seed layer 216 on the first layer of copper, or first level of copper vias 210 and the top surface 214 of the first patterned photoresist layer 208 includes depositing a thin film of Copper (Cu). As before, the second seed layer 216 is deposited to have a thickness of less than 15 nanometers (nm). In one exemplary embodiment, the second seed layer 216 is deposited to form a barely continuous film in the thickness range of 3 to 10 nm. In another exemplary embodiment, the second seed layer 216 is deposited such that the second seed layer 216 possesses a discontinuous island structure 216 having an island thickness in the range of 3 to 10 nm.

In one embodiment, the second seed layer 216 is deposited using a physical vapor deposition process. For example, in one embodiment, the second seed layer 216 is deposited using a sputtering deposition technique. In another embodiment, the second seed layer 216 is deposited using an evaporation deposition technique. One of ordinary skill in the art will understand, upon reading this disclosure, the manner in which such physical vapor deposition processes can be performed to form the second seed layer 216 described herein.

A second patterned photoresist layer 218 is deposited above the second seed layer 216, which defines a number of conductor line openings 220-1, 220-2, . . . , 220-N. In one embodiment, depositing the second patterned photoresist layer 218 which defines a number of conductor line openings 220-1, 220-2, . . . , 220-N, or first level metal line openings 220-1, 220-2, . . . , 220-N. In one embodiment, the number of conductor line openings 220-1, 220-2, . . . , 220-N are defined to form a number of conductor line openings 220-1, 220-2, . . . , 220-N having a near minimum width and

spacing. As one of ordinary skill in the art will understand upon reading this disclosure, this insures a sufficient space in the structure for a subsequent removal of the photoresist layers, e.g. first patterned photoresist layer 208, on lower levels. This consideration is described in greater detail in a co-pending, co-filed application, client docket # 99-0673 entitled, "A Multilevel Copper Interconnect with Double Insulation for ULSI." One of ordinary skill in the art will understand upon reading this disclosure, the manner of forming the second patterned photoresist layer 218. For example, a photoresist layer can be deposited over the second seed layer 216 using any suitable technique, e.g. by spin coating. Then the photoresist can be masked, exposed, and washed to define the number of conductor line openings 220-1, 220-2, . . . , 220-N to the second seed layer 216. One of ordinary skill in the art will further understand, upon reading this disclosure, that the thickness of the second patterned photoresist layer 218 is scalable. That is, the deposition of the photoresist layer 218 is controllable such that the photoresist thickness can be set at a predetermined height (h2). Thus, the scalable thickness of the second patterned photoresist layer 218 determines a height (h2), or depth (h2) for the number of conductor line openings 220-1, 220-2, . . . , 220-N. According to the teachings of the present invention, depositing the second patterned photoresist layer 218 includes depositing the second patterned photoresist layer 218 to have a thickness (h2) which is less than a thickness (h1) of the first patterned photoresist layer 208. That is, the thickness (h2) of the second patterned photoresist layer 218, and consequently a depth (h2) of the number of conductor line openings 220-1, 220-2, . . . , 220-N, is thinner than a depth (h1) of the first level of copper vias 210 defined by the thickness (h1) of the first patterned photoresist layer 208. The structure is now as appears in Figure 2D.

Figure 2E illustrates the structure following the next sequence of processing steps. In Figure 2E, another layer of copper, second layer of copper, or first level of conductor lines 224 is deposited or formed in the number of conductor line openings 220-1, 220-2, . . . , 220-N using electroless plating. One of ordinary skill in the art

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will understand upon reading this disclosure the various manner in which this next layer of copper, second layer of copper, or first level of conductor lines 224 can be deposited in the number of conductor line openings 220-1, 220-2, . . . , 220-N using electroless plating. According to the teachings of the present invention, forming this
5 next layer of copper, second layer of copper, or first level of conductor lines 224 includes filling the number of conductor line openings 220-1, 220-2, . . . , 220-N to a top surface 226 of the second patterned photoresist layer 218. According to the teachings of the present invention depositing this next layer of copper, second layer of copper, or first level of conductor lines 224 over the second seed layer 216 is such
10 that this next layer of copper, second layer of copper, or first level of conductor lines 224 form on the second seed layer 216 but not on the second patterned photoresist layer 218. The structure is now as appears in Figure 2E.

Figure 2F illustrates the structure after the following sequence of processing steps. In Figure 2F, according to the teachings of the present invention, the first
15 patterned photoresist layer 208 and the second patterned photoresist layer 218 are removed. In one exemplary embodiment, removing the first patterned photoresist layer 208 and the second patterned photoresist layer 218 includes removing the first patterned photoresist layer 208 and the second patterned photoresist layer 218 using an oxygen plasma etching. According to the teachings of the present invention, the
20 method further includes removing the first and second seed layers 202 and 216 with the photoresist layers 208 and 218 from areas on the substrate 200 which are not beneath the number of copper vias 210 or between the conductive metal lines 224 and the vias 210. As one of ordinary skill in the art will understand from reading this disclosure, this is due the present inventions novel methodology where the seed
25 layers, 202 and 216, are deposited to have a thickness of less than 15 nanometers (nm), thus forming a barely continuous thin film and/or discontinuous island structure. Other suitable techniques for removing the first patterned photoresist layer 208 and the second patterned photoresist layer 218 can similarly be employed.

At this point, a thin diffusion barrier 228 can be formed on the exposed first level of copper vias 210 and first level of conductor lines 224 as well as the remaining, exposed first and second seed layers, 202 and 216 respectively, located between the substrate, vias, and metal lines. According to the teachings of the present invention, forming a thin diffusion barrier 228 includes forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) 228 having a thickness of less than 8 nanometers (nm). In one embodiment, according to the teachings of the present invention, forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) 228 having a thickness of less than 8 nanometers (nm) includes forming a graded composition of WSi_x , where x varies from 2.0 to 2.5, and nitriding the graded composition of WSi_x . The details of forming a thin diffusion barrier 228, as presented above, are further described in detail in a co-filed, co-pending application; attorney docket # 303.648US1, entitled, "Method for Making Copper Interconnects in Integrated Circuits," which is hereby incorporated by reference. The structure is now as appears in Figure 2F.

As one of ordinary skill in the art will understand upon reading this disclosure, forming additional or subsequent layer/levels of conductive vias and metallization lines are also included within the scope of the present invention. In this scenario, the removal of the first patterned photoresist layer 208 and the second patterned photoresist layer 218 can be delayed until these subsequent layer are completed, the invention is not so limited. That is, if subsequent layers are to be fabricated, the steps illustrated in Figure 2F will be delayed and the process will repeat the sequence provided in Figure 2A-2E.

Figure 2G illustrates the forming of subsequent via and metallization layers prior to the process steps of Figure 2F and continuing in sequence after the number of process steps completed in Figure 2E. For example, Figure 2G shows that in forming subsequent conductive via and metallization layers, another seed layer, or third seed layer, 229 is deposited on the second layer of copper, or first level of conductor lines 224 and the top surface 226 of the second patterned photoresist layer

218. In one embodiment, depositing the third seed layer 229 on the second layer of copper, or first level of conductor lines 224 and the top surface 226 of the second patterned photoresist layer 218 includes depositing a thin film of Palladium (Pd). In another embodiment, depositing the third seed layer 229 on the second layer of copper, or first level of conductor lines 224 and the top surface 226 of the second patterned photoresist layer 218 includes depositing a thin film of Copper (Cu). As before, the third seed layer 229 is deposited to have a thickness of less than 15 nanometers (nm). In one exemplary embodiment, the third seed layer 229 is deposited to form a barely continuous film in the thickness range of 3 to 10 nm. In another exemplary embodiment, the third seed layer 229 is deposited such that the third seed layer 229 possesses a discontinuous island structure 229 having an island thickness in the range of 3 to 10 nm.

In one embodiment, the third seed layer 229 is deposited using a physical vapor deposition process. For example, in one embodiment, the third seed layer 229 is deposited using a sputtering deposition technique. In another embodiment, the third seed layer 229 is deposited using an evaporation deposition technique. One of ordinary skill in the art will understand, upon reading this disclosure, the manner in which such physical vapor deposition processes can be performed to form the third seed layer 229 described herein.

In Figure 2G, a third patterned photoresist layer 230 is deposited above the third seed layer 229, which defines a number of via holes, or openings, 232-1, 232-2, . . . , 232-N to the third seed layer 229. One of ordinary skill in the art will understand upon reading this disclosure, the manner of forming the third patterned photoresist layer 230. For example, a photoresist layer can be deposited over the third seed layer 229 using any suitable technique, e.g. by spin coating. Then the photoresist can be masked, exposed, and washed to define the number of via holes, or openings, 232-1, 232-2, . . . , 232-N to the third seed layer 229. One of ordinary skill in the art will further understand, upon reading this disclosure, that the thickness of the second patterned photoresist layer 218 is scalable. That is, the

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deposition of the photoresist layer 230 is controllable such that the photoresist thickness can be set at a predetermined height (h3). Thus, the scalable thickness of the second patterned photoresist layer 230 determines a height (h3) for the number of via holes, or openings, 232-1, 232-2, . . . , 232-N. The structure is now as appears in Figure 2G.

Figure 2H illustrates the structure continuing on from the process steps included in Figure 2G. In Figure 2H, another layer of copper, third layer of copper, or second level of copper vias 234 is deposited or formed over the third seed layer 229 using electroless plating. One of ordinary skill in the art will understand upon reading this disclosure the various manner in which the third layer of copper, or second level of copper vias 234 can be deposited over the third seed layer 229 using electroless plating. According to the teachings of the present invention, the third layer of copper, or second level of copper vias 234 is formed in the number of via holes, or openings, 232-1, 232-2, . . . , 232-N to the third seed layer 229. Forming the third layer of copper, or second level of copper vias 234 includes filling the number of via holes, or openings, 232-1, 232-2, . . . , 232-N to a top surface 236 of the third patterned photoresist layer 230. According to the teachings of the present invention, depositing third layer of copper, or second level of copper vias 234 over the third seed layer 229 is such that the third layer of copper, or second level of copper vias 234 form on the third seed layer 229 but not on the third patterned photoresist layer 230. The structure is now as appears in Figure 2H.

Figure 2I illustrates the structure following the next sequence of processing steps. In Figure 2I, another seed layer, or fourth seed layer, 238 is deposited on the third layer of copper, or second level of copper vias 234 and the top surface 236 of the third patterned photoresist layer 230. In one embodiment, depositing the fourth seed layer 238 on the third layer of copper, or second level of copper vias 234 and the top surface 236 of the third patterned photoresist layer 230 includes depositing a thin film of Palladium (Pd). In another embodiment, depositing the fourth seed layer 238 on the third layer of copper, or second level of copper vias 234 and the top

surface 236 of the third patterned photoresist layer 230 includes depositing a thin film of Copper (Cu). As before, the fourth seed layer 238 is deposited to have a thickness of less than 10 nanometers (nm). In one exemplary embodiment, the fourth seed layer 238 is deposited to form a barely continuous film in the thickness
5 range of 3 to 10 nm. In another exemplary embodiment, the fourth seed layer 238 is deposited such that the fourth seed layer 238 possesses a discontinuous island structure 238 having an island thickness in the range of 3 to 10 nm.

In one embodiment, the fourth seed layer 238 is deposited using a physical vapor deposition process. For example, in one embodiment, the fourth seed layer
10 238 is deposited using a sputtering deposition technique. In another embodiment, the fourth seed layer 238 is deposited using an evaporation deposition technique. One of ordinary skill in the art will understand, upon reading this disclosure, the manner in which such physical vapor deposition processes can be performed to form the fourth seed layer 238 described herein.

15 A fourth patterned photoresist layer 240 is deposited above the fourth seed layer 238, which defines a number of conductor line openings 242-1, 242-2, . . . , 242-N. In one embodiment, depositing the fourth patterned photoresist layer 240 which defines a number of conductor line openings 242-1, 242-2, . . . , 242-N includes defining a number of second level metal line openings 242-1, 242-2, . . . ,
20 242-N. In one embodiment, the second number of conductor line openings 242-1, 242-2, . . . , 242-N are defined to form a number of conductor line openings 242-1, 242-2, . . . , 242-N having a near minimum width and spacing. As one of ordinary skill in the art will understand upon reading this disclosure, this insures a sufficient space in the structure for a subsequent removal of the photoresist layers, e.g. first,
25 second, and third patterned photoresist layer 208, 218, and 230 on lower levels. This consideration is described in greater detail in a co-pending, co-filed application, client docket # 99-0673 entitled, "A Multilevel Copper Interconnect with Double Insulation for ULSI." One of ordinary skill in the art will understand upon reading this disclosure, the manner of forming the fourth patterned photoresist layer 240.

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For example, a photoresist layer can be deposited over the fourth seed layer 238 using any suitable technique, e.g. by spin coating. Then the photoresist can be masked, exposed, and washed to define the number of conductor line openings 242-1, 242-2, . . . , 242-N to the fourth seed layer 238. One of ordinary skill in the art will further understand, upon reading this disclosure, that the thickness of the fourth patterned photoresist layer 240 is scalable. That is, the deposition of the fourth patterned photoresist layer 240 is controllable such that the photoresist thickness can be set at a predetermined height (h4). Thus, the scalable thickness of the fourth patterned photoresist layer 240 determines a height (h4) for the number of conductor line openings 242-1, 242-2, . . . , 242-N. According to the teachings of the present invention, depositing the fourth patterned photoresist layer 240 includes depositing the fourth patterned photoresist layer 240 to have a thickness (h4) which is less than a thickness (h3) of the third patterned photoresist layer 230. That is, the thickness (h3) of the third patterned photoresist layer 230 is thinner than a depth (h3) of the second level of copper vias 234 defined by the thickness (h3) of the third patterned photoresist layer 230. The structure is now as appears in Figure 2I.

Figure 2J illustrates the structure following the next sequence of processing steps. In Figure 2E, another layer of copper, fourth layer of copper, or second level of conductor lines 244 is deposited or formed in the number of conductor line openings 242-1, 242-2, . . . , 242-N using electroless plating. One of ordinary skill in the art will understand upon reading this disclosure the various manner in which this fourth layer of copper, or second level of conductor lines 244 can be deposited in the number of conductor line openings 242-1, 242-2, . . . , 242-N using electroless plating. According to the teachings of the present invention, forming this fourth layer of copper, or second level of conductor lines 244 includes filling the number of conductor line openings 242-1, 242-2, . . . , 242-N to a top surface 246 of the fourth patterned photoresist layer 240. According to the teachings of the present invention depositing this fourth layer of copper, or second level of conductor lines 244 over the fourth seed layer 238 is such that this fourth layer of copper, or second level of

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conductor lines 244 form on the fourth seed layer 238 but not on the fourth patterned photoresist layer 240. The structure is now as appears in Figure 2J.

Figure 2K illustrates the structure after the following sequence of processing steps. In Figure 2K, according to the teachings of the present invention, the first, second, third, and fourth patterned photoresist layers 208, 218, 230, and 240 are removed. In one exemplary embodiment, removing the first, second, third, and fourth patterned photoresist layers 208, 218, 230, and 240 includes removing the first, second, third, and fourth patterned photoresist layers 208, 218, 230, and 240 using an oxygen plasma etching. According to the teachings of the present invention, the method further includes removing the first, second, third, and fourth seed layers, 202, 216, 229 and 238 respectively, with the photoresist layers from areas on the substrate which are not beneath the number of copper vias or between the conductive metal lines and the vias. As one of ordinary skill in the art will understand from reading this disclosure, this is due the present inventions novel methodology where the seed layers, 202, 216, 229 and 238, are deposited to have a thickness of less than 15 nanometers (nm), thus forming a barely continuous thin film and/or discontinuous island structure. Other suitable techniques for removing the first, second, third, and fourth patterned photoresist layers 208, 218, 230, and 240 can similarly be employed. As one of ordinary skill in the art will further understand upon reading this disclosure, the first, second, third, and fourth patterned photoresist layers 208, 218, 230, and 240 can be removed at earlier or later stages of a fabrication process, as described herein, depending on the number of via and metal levels to be formed.

At this point, or as could equally be performed at an earlier or later stage depending on when the photoresist layers are removed, a thin diffusion barrier 248 can be formed on the exposed first and second level of copper vias 210, 234 and the exposed first and second level of conductor lines 224, 244 as well as the remaining, exposed first, second, third, and fourth seed layers, 202, 216, 229 and 238 respectively, located between the substrate, vias, and metal lines. According to the

teachings of the present invention, forming a thin diffusion barrier 248 includes forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) 248 having a thickness of less than 8 nanometers (nm). In one embodiment, according to the teachings of the present invention, forming a thin diffusion barrier of Tungsten Silicon Nitride (WSi_xN_y) 248 having a thickness of less than 8 nanometers (nm) includes forming a graded composition of WSi_x , where x varies from 2.0 to 2.5, and nitriding the graded composition of WSi_x . The details of forming a thin diffusion barrier 228, as presented above, are further described in detail in a co-filed, co-pending application; attorney docket # 303.648us1, entitled, "Method for Making Copper Interconnects in Integrated Circuits," which is hereby incorporated by reference. The structure is now as appears in Figure 2K.

Structure

Figure 3 is an illustration of an integrated circuit 300 formed according to the teachings of the present invention. According to the teachings of the present invention, the integrated circuit 300 includes a multilayer copper wiring structure. As shown in Figure 3, the integrated circuit 300 includes at least one semiconductor device 301 formed in a substrate 302. A first number of seed layers 304-1, 304-2, . . . , 304-N are formed on a number of portions 305-1, 305-2, . . . , 305-N of the at least one semiconductor device. As one of ordinary skill in the art will understand upon reading this disclosure the number of portions 305-1, 305-2, . . . , 305-N of the at least one semiconductor device 301 include the number of portions 305-1, 305-2, . . . , 305-N of a semiconductor device 301 which require electrical contact to subsequent integrated circuit layers formed above the semiconductor device 301. For example, the at least one semiconductor device 301 can include at least one transistor 301 which has a source and a drain region. In this scenario, the number of portions 305-1, 305-2, . . . , 305-N of a semiconductor device 301 which require electrical contact to subsequent integrated circuit layers formed above the

semiconductor device 301 include the source and the drain regions 305-1, 305-2, . . ., 305-N.

As shown in Figure 3, a number of copper vias 307-1, 307-2, . . ., 307-N, or first level of copper vias 307-1, 307-2, . . ., 307-N, are formed above and contact
5 with the first number of seed layers 304-1, 304-2, . . ., 304-N. According to the teachings of the present invention, the first number of seed layers 304-1, 304-2, . . ., 304-N include a thin film of Palladium (Pd) or Copper. Further, the first number of seed layers 304-1, 304-2, . . ., 304-N have a thickness of less than 15 nanometers (nm). In one embodiment, the first number of seed layers 304-1, 304-2, . . ., 304-N
10 includes a first number of seed layers 304-1, 304-2, . . ., 304-N having a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

A second number of seed layers 309-1, 309-2, . . ., 309-N are formed on the number of copper vias 307-1, 307-2, . . ., 307-N. According to the teachings of the
15 present invention, the second number of seed layers 309-1, 309-2, . . ., 309-N include a thin film of Palladium (Pd) or Copper. Further, the second number of seed layers 309-1, 309-2, . . ., 309-N have a thickness of less than 15 nanometers (nm). In one embodiment, the second number of seed layers 309-1, 309-2, . . ., 309-N includes a second number of seed layers 309-1, 309-2, . . ., 309-N having a
20 discontinuous island structure with an island thickness in the range of 3 to 10 nanometers.

A number of conductor metal lines 311-1, 311-2, . . ., 311-N, or first level of conductor metal lines 311-1, 311-2, . . ., 311-N, are formed above and contact with the second number of seed layers 309-1, 309-2, . . ., 309-N. In one embodiment, the
25 first level of conductor metal lines 311-1, 311-2, . . ., 311-N includes a number of copper metal lines 311-1, 311-2, . . ., 311-N. In one embodiment, as shown in Figure 3, the integrated circuit 300 further includes a thin diffusion barrier 315 covering the number of copper vias 307-1, 307-2, . . ., 307-N, the number of

conductor metal lines 311-1, 311-2, . . . , 311-N, and the first and the second number of seed layers, 304-1, 304-2, . . . , 304-N, and 309-1, 309-2, . . . , 309-N respectively. According to the teachings of the present invention, the thin diffusion barrier 315 has a thickness of less than 8.0 nanometers (nm). In one embodiment, the thin
5 diffusion barrier has a thickness in the range of 2.0 to 6.0 nanometers. In one embodiment, the thin diffusion barrier 315 includes a graded composition of Tungsten Silicon Nitride (WSi_xN_y), and wherein x varies from 2.0 to 2.5.

In one embodiment, as shown in Figure 3, the integrated circuit, or multilayer copper wiring structure 300 includes a third number of seed layers 317-1,
10 317-2, . . . , 317-N, including a thin film of Palladium (Pd) or Copper, are formed on the first level of copper metal lines 311-1, 311-2, . . . , 311-N, or first level of conductor metal lines 311-1, 311-2, . . . , 311-N. Further, the third number of seed layers 317-1, 317-2, . . . , 317-N have a thickness of less than 15 nanometers (nm). In one embodiment, the third number of seed layers 317-1, 317-2, . . . , 317-N
15 includes a third number of seed layers 317-1, 317-2, . . . , 317-N having a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers. A second level of copper vias 319-1, 319-2, . . . , 319-N are formed above and contacting the third number of seed layers 317-1, 317-2, . . . , 317-N. A fourth number of seed layers 321-1, 321-2, . . . , 321-N, including a thin film of
20 Palladium (Pd) or Copper, are formed on the second level of copper vias 319-1, 319-2, . . . , 319-N. In one embodiment, the fourth number of seed layers 321-1, 321-2, . . . , 321-N includes a fourth number of seed layers 321-1, 321-2, . . . , 321-N having a discontinuous island structure with an island thickness in the range of 3 to 10 nanometers. A second level of copper metal lines 323-1, 323-2, . . . , 323-N, or
25 second level of conductor metal lines 323-1, 323-2, . . . , 323-N, are formed above and contacting fourth number of seed layers 321-1, 321-2, . . . , 321-N.

In one embodiment, as shown in Figure 3, the thin diffusion barrier 315 further covers the second level of copper vias 319-1, 319-2, . . . , 319-N, the second level of copper metal lines 323-1, 323-2, . . . , 323-N, and the third, and fourth

number of seed layers, 317-1, 317-2, . . . , 317-N and 321-1, 321-2, . . . , 321-N respectively.

Conclusion

5 Thus, structures and methods have been shown which include a selective electroless copper metallization. The present invention provides for a multilayer copper wiring structure by electroless, selectively deposited copper which will not require chemical mechanical planarization (CMP). Thus, the present invention is streamlined and significantly reduces the amount of deposited conductive material,
10 e.g. copper, which is ultimately discarded according to conventional processes. This also alleviates important environmental concerns regarding the disposition of used materials. Further, by avoiding the need for a CMP process step the usage of consumables such as pads and slurry is conserved.

 Although specific embodiments have been illustrated and described herein, it
15 will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiment shown. This application is intended to cover any adaptations or variations of the present invention. It is to be understood that the above description is intended to be illustrative, and not restrictive. The scope of the invention includes
20 any other applications in which the above structures and fabrication methods are used. The scope of the invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.